REMARKS

Claims 1-9 are pending. Claims 1-9 are rejected. Claims 1, 3-5, and 7-8 are amended. Claims 6 and 9 are cancelled. Claims 10-18 are added. In view of the amendments, Applicant respectfully requests reconsideration of this application.

Rejection Under 35 U.S.C. § 102(b)

In paragraph 1 of the Office Action, the Examiner rejected claim 9 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,726,584 to Freidin. Because Applicant has canceled claim 9, the rejection of claim 9 under 35 U.S.C. § 102(b) is now moot.

Rejection Under 35 U.S.C. § 103(a)

In paragraph 2 of the Office Action, the Examiner rejected claims 1-8 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 5,414,377 to Freidin (hereinafter Freidin '377). The Examiner stated, "Freidin discloses a programmable logic device...that provide [sic] a result logic value (see X, Y in Fig. 3) in response to one or more input logic values (see C0-7 in Fig. 7 [sic—should be "Fig. 3"]) and a function vector (see S1 in Fig. 3)...."

In contrast to the assertion of the Examiner, Freidin '377 does not teach or suggest all elements of amended (or original) claim 1. In particular, items C0-7 of Fig. 3 in Freidin '377 are not "input logic values," and S1 of Fig. 3 is not "a function vector." Applicant notes that Freidin '377 is directed to "using ***memory bits in a look-up table to provide any function of several inputs***...the ***memory bits***...***serv***[*e*] ***as a look-up table to generate a function, and control***[] ***gates***...***to generate*** a function" (Abstract, emphasis added).

With respect to the input logic values, stated by the Examiner to be taught by C0-7, Freidin '377 states, "FIG. 3 shows a logic block according to the present invention in which...the logic block...provid[es] a ***function of four variables, A, B, C, and D***...[or] a ***function of three variables, for example A, B, and C...*** Memory cells 108a through 108h [fed by lines C0-7] provide the dual function of generating a function of three of the four variables A, B, C, and D or of configuring certain of the multiplexers in the remainder of the logic block" (col. 3, lines 58-67, emphasis added). Therefore, the input logic values of Fig. 3 in Freidin '377 are A, B, C, and D, and not C0-7. C0-7 of Fig. 3 in Freidin '377 merely program the look-up table to provide a function of the input logic values.

Further, with respect to S1 of Fig. 3 in Freidin '377, S1 is not "a function vector," as stated by the Examiner. Freidin '377 states, "FIG. 3 shows a logic block according to the present invention in which additional [single-bit] ***memory cell S1*** indicates whether the logic block is to be used in its default mode, ...or ...configured in a user selected configuration" (col. 3, lines 58-67, emphasis added). Fig. 3 of Freidin '377 shows that ***S1 is a single-bit memory cell with a single-bit output***. S1 of Freidin '377 cannot be a function ***vector*** because S1 is a single-bit (scalar) quantity stored in a memory cell.

Regardless, Freidin '377 provides merely look-up tables of pre-programmed functions. As described in the prior art section of the present application, one problem of such look-up table structures is that ***the look-up table can only be statically programmed*** to perform different levels of functionality. In contrast, amended claim 1 now includes, "a plurality of function cells, each of the function cells configured to provide a result logic value in response to one or more input logic values and a ***static or dynamic*** function vector" (emphasis added). Freidin '377 does not disclose or suggest that the function vector may be static or dynamic.

Furthermore, amended claim 1 now includes, "each of the function cells having an arithmetic logic circuit that in a first mode is operable to provide the result logic value as a first arithmetic combination of the input logic values and in a second mode is operable to provide the result logic value as a second arithmetic combination of the input logic values, the first arithmetic combination and the second arithmetic combination determined by the function vector, the first mode and the second mode ***selected by a global function select signal coupled to at least two of the plurality of function cells***" (emphasis added). Freidin '377 does not disclose or suggest a global function select signal coupled to at least two of the plurality of function cells to select the first mode and the second mode.

With respect to the dependent claims, claims 2-5 and 7-8 depend directly from claim 1 and are therefore allowable for at least the same reasons as claim 1.

Applicant notes that no new matter is added with this amendment. Support for the claim amendments and new claims is found in the detailed description at least at pages 10-12 and 18-19.

CONCLUSION

Applicants believe that the rejections and objections in the Office Action of April 9, 2004 are fully overcome and that the application is in condition for allowance. If the Examiner has any questions regarding the case, the Examiner is invited to contact Applicants' undersigned representative at the number given below.

Respectfully submitted,

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